Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 13, with the following amended paragraph:

A known implementation of the frequency detector is the quadricorrelator concept as in "Digital Logic Implementation of Quadricorrelators for Frequency detectors", by C. G. Yoon, S. Y. Lee and C. W. Lee, IEEE Proc. of 37.sup.th MidWest Symposium on Circuits and Systems, 1994, pp. 757-760. A model for a balanced digital quadricorrelator is a balanced analog quadricorrelator as shown in FIG. 1. The analog quadricorrelator comprises a first pair of mixers M1, M2 supplied by quadrature signals I, Q and input signal IN. Outputs of said pair of mixers M1, M2 are coupled to a pair of low-pass filters L1, L2, the filters providing signals Vi and Vq, respectively. The signals Vi and Vq are inputted to a pair of derivation circuits D1, D2 coupled to a second pair of mixers M3, M4 and crossed-inputted to the second pair of mixers M3, M4. Signals provided by the second pair of mixers are inputted to an adder S. The adder S provides a signal FD, which is indicative for a frequency error between the input signal IN and quadrature signals I, Q. In the above-mentioned document is presented a digital implementation of the analog balanced quadricorrelator. The digital implementation comprises single edge flip-flops coupled to a combinatorial network. Hence the flip-flops detects only phase shifts between quadrature inputs and a rising edge of the D input signal, which means that this quadricorrelator works at half rate or 2*Tbit. Tbit is defined as the time period for a high or a low binary level. Furthermore, the combinatorial part of the quadricorrelator comprises ~~8 AND 3-input gates and 2 OR 4-input gates~~ eight 3-input AND gates and two 4-input OR gates determining delays and supplementary phase-shifts between the signals provided by the quadricorrelator determined by technological errors in matching components.

Please replace the paragraph beginning on page 2, line 21, with the following amended paragraph:

In an embodiment of the invention a first pair of double edge clocked bi-stable circuits coupled to a first multiplexer and a second pair of double edge clocked bi-stable circuits coupled to a second multiplexer are supplied by mutually quadrature phase shifted signals respectively. The first multiplexer and the second multiplexer provide a first signal and a second signal indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals. The mutually quadrature phase shifted signals are generated by a voltage controlled oscillator. In many applications ~~as optical networking~~ such as optical networking, a clock recovery is necessary especially when the clock information in missing from the input signal as in Non Return to Zero (NRZ) signals. Furthermore, clock recovery circuits use normally a PLL, the PLL having a quadrature voltage-controlled oscillator providing quadrature signals i.e. mutually shifted with 45 degrees. PLLs also have a phase detector and a frequency detector. The outputs of the multiplexers are updated only on the transitions of the incoming signal maintaining the same error at the output between transitions. The phase difference between the incoming signal and quadrature clock signals is transformed in a positive or negative quantified signal. When this signal is positive the clock increases its phase and for negative signals, the clock decreases its phase.

Please replace the paragraph beginning on page 4, line 24, with the following amended paragraph:

The combination latch-multiplexer performs as a latch clocked on both transitions of the incoming signal D. The incoming signal D transitions are sampled by the two quadrature signals CKI and CKQ at Tbit rate. The outputs of the multiplexers are updated only on the incoming signal D transitions keeping the same error at the output between transitions. The second output signal Q is the output of the phase detector and the first of the output signals I is in quadrature with Q. The phase difference between the incoming signal D and ~~CKQ, respectively CKI~~ the mutually quadrature phase shifted signals CKI

and CKQ, respectively, is transformed in a positive or negative quantified signal. When this signal is positive the clock increases its phase and for negative signals, the clock decreases its phase. The third and fourth pairs of latches 25, 26, 27, 28 are sampled on the transitions of I and Q signals. It is observed a sign inversion of the outputs of the latches sampling I and Q outputs on positive values of Q and I respectively. The inversion is needed to duplicate the working principle of a differentiator, which gives positive values on the rising edge and negative values on the falling edge of a signal. An alternative version of the quadricorrelator without inversion produces a frequency error too but the gain of the frequency detector decreases accordingly (only one transition is used for comparison).